

Features

- **HIGH PERFORMANCE E²CMOS[®] TECHNOLOGY**
 - 10 ns Maximum Propagation Delay
 - F_{max} = 166 MHz
 - 7ns Maximum from Clock Input to Data Output
 - TTL Compatible 12 mA Outputs
 - UltraMOS[®] Advanced CMOS Technology
- **ACTIVE PULL-UPS ON ALL PINS**
- **COMPATIBLE WITH STANDARD 22V10 DEVICES**
 - Fully Function/Fuse-Map/Parametric Compatible with Bipolar and UVC MOS 22V10 Devices
- **50% REDUCTION IN POWER VERSUS BIPOLAR**
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **TEN OUTPUT LOGIC MACROCELLS**
 - Maximum Flexibility for Complex Logic Designs
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
 - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

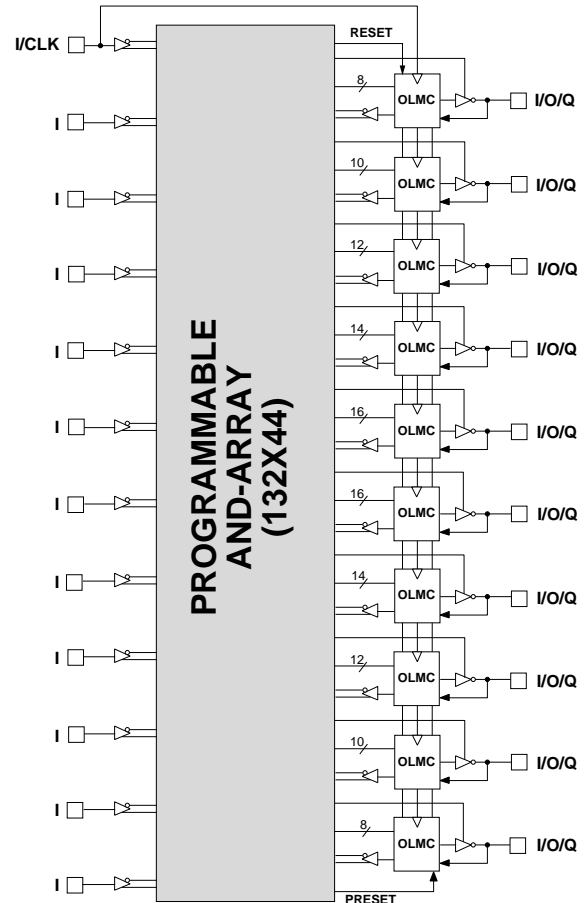
Description

The GAL22V10/883 is a high performance E²CMOS programmable logic device processed in full compliance to MIL-STD-883. This military grade device combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed performance available of any military qualified 22V10 device. CMOS circuitry allows the GAL22V10 to consume much less power when compared to bipolar 22V10 devices. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

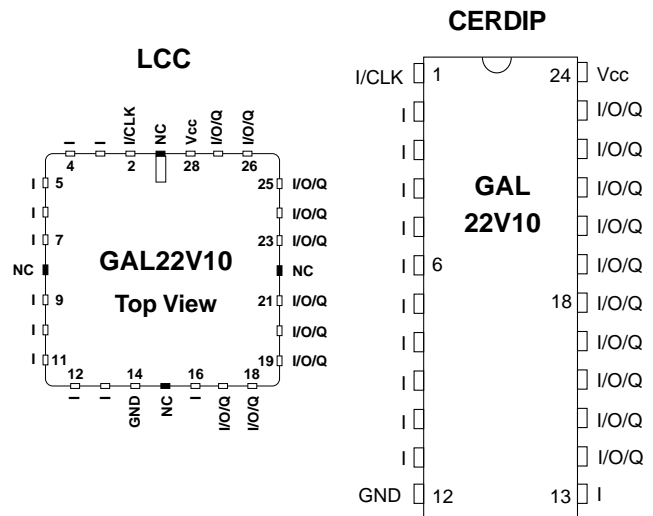
The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL22V10 is fully function/fuse map/parametric compatible with standard bipolar and CMOS 22V10 devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Functional Block Diagram



Pin Configuration



Copyright © 1999 Lattice Semiconductor Corp. All brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Absolute Maximum Ratings⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Case Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

Case Temperature (T_C) -55 to 125°C
 Supply Voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS	
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V	
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V	
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA	
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA	
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V	
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V	
I_{OL}	Low Level Output Current		—	—	12	mA	
I_{OH}	High Level Output Current		—	—	-2.0	mA	
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-50	—	-135	mA	
I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz \text{ Outputs Open}$	L -10/-15/-20/-25/-30	—	90	150	mA

- 1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
- 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Characterized but not 100% tested.
- 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$.

AC Switching Characteristics

Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	-10		-15		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinatorial Output	—	10	—	15	ns
t_{co}	A	Clock to Output Delay	—	7	—	8	ns
t_{cf}²	—	Clock to Feedback Delay	—	7	—	8	ns
t_{su}	—	Setup Time, Input or Feedback before Clock [↑]	6	—	12	—	ns
t_h	—	Hold Time, Input or Feedback after Clock [↑]	0	—	0	—	ns
f_{max}³	A	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	76.9	—	50	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	76.9	—	50	—	MHz
	A	Maximum Clock Frequency with No Feedback	166	—	62.5	—	MHz
t_{wh}	—	Clock Pulse Duration, High	3	—	8	—	ns
t_{wl}	—	Clock Pulse Duration, Low	3	—	8	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	10	—	15	ns
t_{dis}	C	Input or I/O to Output Disabled	—	12	—	15	ns
t_{ar}	A	Input or I/O to Asynchronous Reset of Register	—	12	—	20	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	10	—	15	—	ns
t_{arr}	—	Asynchronous Reset to Clock Recovery Time	6	—	15	—	ns
t_{spr}	—	Synchronous Preset to Clock Recovery Time	10	—	12	—	ns

1) Refer to **Switching Test Conditions** section.

2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Description** section.

3) Refer to **f_{max} Description** section.

Capacitance (TA = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C _I	Input Capacitance	10	pF	V _{CC} = 5.0V, V _I = 2.0V
C _{I/O}	I/O Capacitance	10	pF	V _{CC} = 5.0V, V _{I/O} = 2.0V

*Characterized but not 100% tested.

AC Switching Characteristics

Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	-20		-25		-30		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinatorial Output	—	20	—	25	—	30	ns
t_{co}	A	Clock to Output Delay	—	15	—	20	—	20	ns
t_{cf}²	—	Clock to Feedback Delay	—	15	—	20	—	20	ns
t_{su}	—	Setup Time, Input or Feedback before Clock [↑]	17	—	20	—	25	—	ns
t_h	—	Hold Time, Input or Feedback after Clock [↑]	0	—	0	—	0	—	ns
f_{max}³	A	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	31.2	—	25	—	22	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	31.2	—	25	—	22	—	MHz
	A	Maximum Clock Frequency with No Feedback	33	—	33	—	25	—	MHz
t_{wh}	—	Clock Pulse Duration, High	15	—	15	—	20	—	ns
t_{wl}	—	Clock Pulse Duration, Low	15	—	15	—	20	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	20	—	25	—	25	ns
t_{dis}	C	Input or I/O to Output Disabled	—	20	—	25	—	25	ns
t_{ar}	A	Input or I/O to Asynchronous Reset of Register	—	25	—	30	—	30	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	20	—	25	—	30	—	ns
t_{arr}	—	Asynchronous Reset to Clock Recovery Time	20	—	25	—	30	—	ns
t_{spr}	—	Synchronous Preset to Clock Recovery Time	17	—	20	—	25	—	ns

1) Refer to **Switching Test Conditions** section.

2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Description** section.

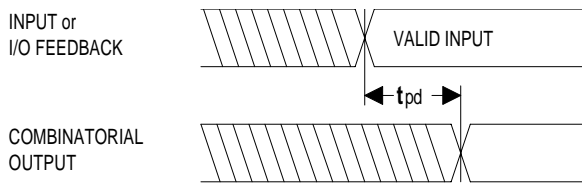
3) Refer to **f_{max} Description** section.

Capacitance (T_A = 25°C, f = 1/0 MHz)

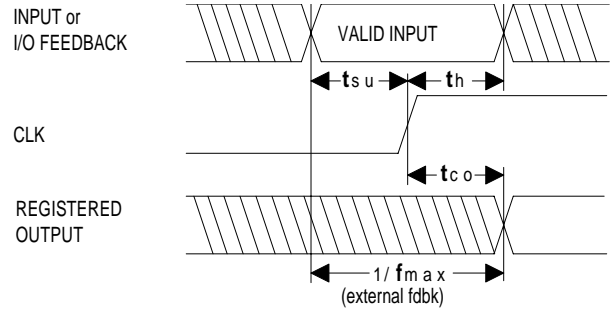
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C _I	Input Capacitance	10	pF	V _{CC} = 5.0V, V _I = 2.0V
C _{I/O}	I/O Capacitance	10	pF	V _{CC} = 5.0V, V _{I/O} = 2.0V

*Characterized but not 100% tested.

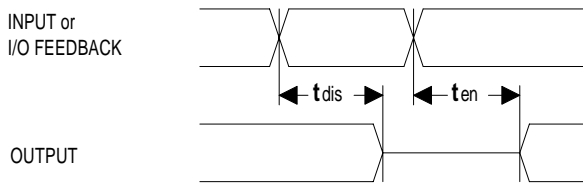
Switching Waveforms



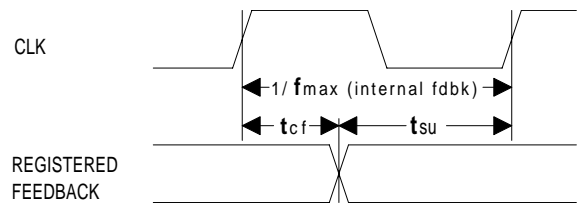
Combinatorial Output



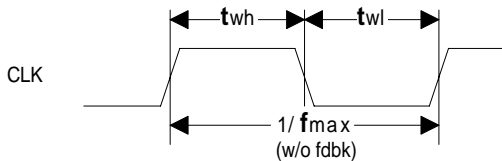
Registered Output



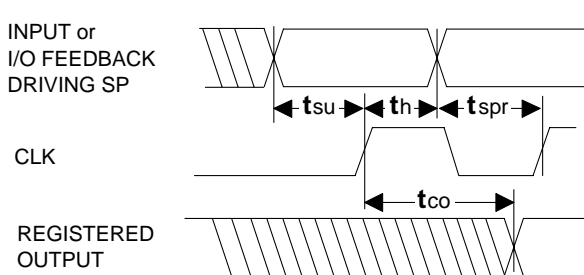
Input or I/O to Output Enable/Disable



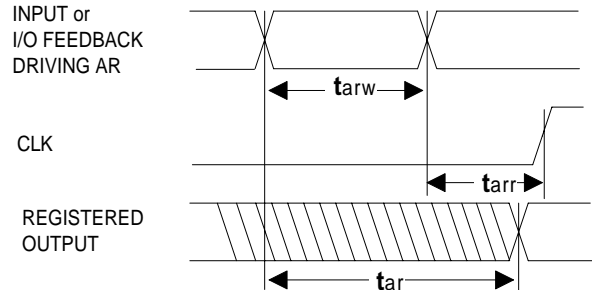
fmax with Feedback



Clock Width

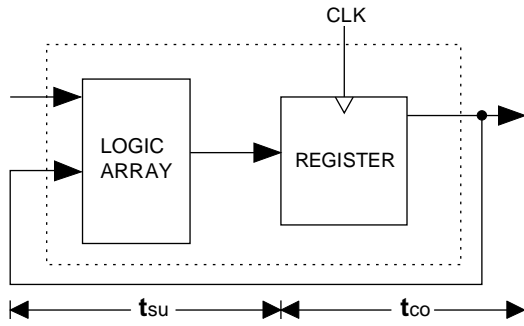


Synchronous Preset



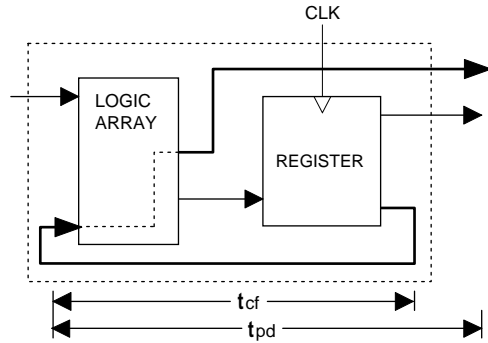
Asynchronous Reset

f_{max} Descriptions



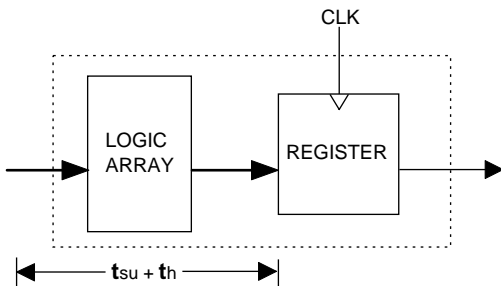
f_{max} with External Feedback 1/(t_{su}+t_{co})

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with Internal Feedback 1/(t_{su}+t_{cf})

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/internal feedback (t_{cf} = 1/f_{max} - t_{su}). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to t_{cf} + t_{pd}.



f_{max} with No Feedback

Note: f_{max} with no feedback may be less than 1/(t_{wh} + t_{wl}). This is to allow for a clock duty cycle of other than 50%.

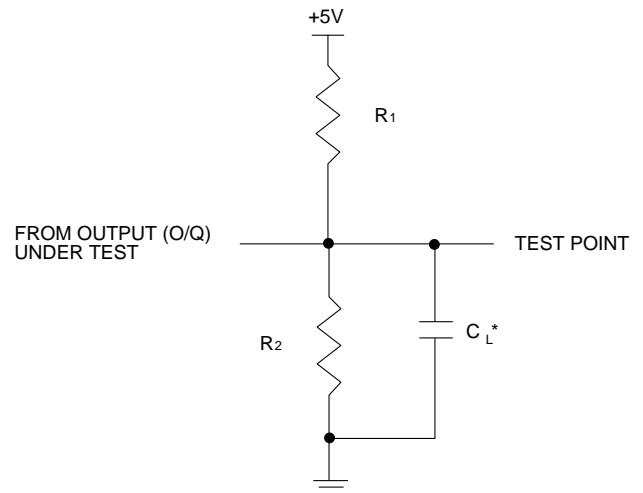
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
A	390Ω	750Ω	50pF
B	Active High	∞	750Ω
	Active Low	390Ω	750Ω
C	Active High	∞	5pF
	Active Low	390Ω	750Ω



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

GAL22V10 Ordering Information (MIL-STD-883 and SMD)

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Package	Ordering #	
					MIL-STD-883	SMD #
10	6	7	150	24-Pin CERDIP	GAL22V10D-10LD/883	5962-8984106LA
				28-Pin LCC	GAL22V10D-10LR/883	5962-89841063A
15	12	8	150	24-Pin CERDIP	GAL22V10D-15LD/883	5962-8984103LA
				28-Pin LCC	GAL22V10D-15LR/883	5962-89841033A
20	17	15	150	24-Pin CERDIP	GAL22V10D-20LD/883	5962-8984102LA
				28-Pin LCC	GAL22V10D-20LR/883	5962-89841023A
25	20	20	150	24-Pin CERDIP	GAL22V10D-25LD/883	5962-8984104LA
30	25	20	150	24-Pin CERDIP	GAL22V10D-30LD/883	5962-8984101LA

Note: Lattice Semiconductor recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number is recommended.

Part Number Description

